IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Matthew J. Adiletta et al. Art Unit :
Serial No. : Examiner :
Filed :
Title : FUNCTIONAL PIPELINES

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as follows:

In the claims:

Amend claims 1, 5, 16, 17, 18, 21, and 22 as follows:

--1. (Amended) A system comprising:

a parallel processor that assigns system functions for processing data, the parallel processor comprising:

a plurality of programming engines that support multiple contexts, the plurality of programming engines arranged to provide a functional pipeline; and

a functional pipeline control unit that assigns system function and passes functional data among the plurality of programming engines.

5. (Amended) The system of claim 4 wherein each of the plurality of functional pipeline stages performs a different system function.

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Typed or Printed Name of Person Signing Certificate

16. (Amended) A method of transferring data between a plurality of programming engines, the method comprising:

assigning system functions for processing data to corresponding ones of a plurality of programming engines that provide a functional pipeline unit in a parallel processor and, which supports execution of multiple contexts in each of the plurality of programming engines; and

passing functional data among the plurality of programming engines in the functional pipeline unit.

17. (Amended) The method of claim 16 further comprising:

synchronizing the system functions across the functional pipeline unit.

18. (Amended) The method of claim 17 further comprising:

partitioning an execution time into a number of time intervals corresponding to the number of plurality of pipeline stages.

21. (Amended) The method of claim 16 further comprising:

using a critical section that provides exclusive access for the multiple contexts to non-shared data required for processing data packets.

22. (Amended) The method of claim 16 further comprising:

employing an elasticity buffer to accommodate jitter between the plurality of pipeline stages upon execution of a data packet processing function.--

REMARKS

Applicants have amended the application to correct minor typographical errors in the claims.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be examined. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 1-17-02

Scott C. Harris
Reg. No. 32,030

Fish & Richardson P.C.
4350 La Jolla Village Drive, Suite 500
San Diego, California 92122
Telephone: 858 678-5070
Facsimile: 858 678-5099

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Version with markings to show changes made

In the claims:

Claims 1, 5, 16, 17, 18, 21, and 22 have been amended as follows:

1. (Amended) A system comprising:

a parallel processor that assigns system functions for processing data [including], the parallel processor comprising:

a plurality of programming engines that support multiple contexts, the plurality of programming engines arranged to provide a functional pipeline; and [by]

a functional pipeline control unit that assigns system function and passes functional data among the plurality of programming engines.

5. (Amended) The system of claim 4 wherein each of the plurality of functional pipeline stages performs a different system function.

16. (Amended) A method of transferring data between a plurality of programming engines, the method comprising:

assigning system functions for processing data [in a parallel processor] to corresponding ones of a plurality of programming engines that provide a functional pipeline unit in a parallel processor and, which supports execution of multiple contexts in each of the plurality of programming engines; and

passing functional data among the plurality of programming engines in the functional pipeline unit.

17. (Amended) The method of claim 16 further comprising:

synchronizing the system functions across the functional pipeline unit.

18. (Amended) The method of claim 17 further comprising:

partitioning an execution time into a number of time intervals corresponding to the number of plurality of pipeline stages.

21. (Amended) The method of claim 16 further comprising:

using a critical section that provides exclusive access for the multiple contexts to non-shared data required for processing data packets.

22. (Amended) The method of claim 16 further comprising:

employing an elasticity buffer to accommodate jitter between the plurality of pipeline stages upon execution of a data packet processing function.--